DECLARATION

I, the undersigned, of 2-12, Nakazaki 2-chome, Kita-ku, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **11-192659**

that was filed in Japanese.

I declare that all statements made herein of may own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

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[Name of Document] Specification

[Title of the Invention] SEMICONDUCTOR ELEMENT, AND METHOD FOR FORMING FILM

[Claims]

[Claim 1] A semiconductor element comprising an insulating film and a conductor electrode on a semiconductor substrate, characterized in that the insulating film is at least partially formed of an AlN layer.

[Claim 2] The semiconductor element according to Claim 1, characterized in that the semiconductor element is a field effect transistor and the insulating film is a gate insulating film of the field effect transistor.

[Claim 3] The semiconductor element according to Claim 1, characterized in that the AlN layer is a single crystal layer epitaxially grown on the substrate.

[Claim 4] The semiconductor element according to Claim 3, characterized in that the plane orientation of principal plane of the semiconductor substrate is the (100) plane, and that the AlN is a cubic crystal of which the plane orientation is the (100) plane.

[Claim 5] The semiconductor element according to Claim 4, characterized in that the semiconductor substrate is formed of Si.

[Claim 6] The semiconductor element according to Claim 5, characterized in that dangling bonds at the surface of the semiconductor substrate are terminated by one of aluminum, nitrogen, hydrogen, sulfur and magnesium.

[Claim 7] The semiconductor element according to Claim 5, characterized in that the insulating film further comprises a silicon nitride layer interposed between the AlN layer and the semiconductor substrate.

[Claim 8] The semiconductor element according to any one of Claims 1 to 7, characterized in that the insulating film further includes a dielectric layer which is formed on the AlN layer and which is made of at least one of a dielectric material with a higher dielectric constant than AlN and a material with ferroelectric properties.

[Claim 9] The semiconductor element according to any one of Claims 1 to 7, characterized in that:

the insulating film further includes a dielectric layer which is formed on the AlN film and which is made of at least one of a dielectric material with a higher dielectric constant than AlN and a material with ferroelectric properties; and

a conductive film with crystallinity is provided at least either above or below the dielectric layer.

[Claim 10] The semiconductor element according to any one of Claims 1 to 7, characterized in that the AlN layer includes at least one of oxygen, hydrogen and sulfur, and strain in the AlN layer resulting from lattice mismatching with the semiconductor substrate is relieved.

[Claim 11] The semiconductor element according to Claim 4, characterized in that the lattice mismatch of the AlN layer with the semiconductor substrate is expanded to increase the dielectric constant of the AlN layer.

[Claim 12] A method for forming a film, characterized by alternately repeating a step (a) of forming either one atom layer of an Al atom layer and an N atom layer on a semiconductor substrate of which the plane orientation of principal plane is the (100) plane, and a step (b) of forming the other atom layer of the Al atom layer and the N atom layer on said one atom layer, thereby forming an AlN layer which is a cubic crystal having the (100) plane.

[Claim 13] The method for forming a film according to Claim 12, characterized in that deposition of the Al atom layer and the N atom layer is performed by a molecular beam epitaxy (MBE) method or metal organic vapor phase epitaxy (MOVPE) method.

[Claim 14] The method for forming a film according to Claim 12 or 13, characterized in an Si substrate is used as the semiconductor substrate.

[Claim 15] The method for forming a film according to any one of Claims 12 to 14, characterized in that:

before the step (a), the step of nitrogenizing the surface of the semiconductor substrate to form a silicon nitride layer is further included; and

in the step (b) said one atom layer is formed on the silicon nitride layer.

[Claim 16] The method for forming a film according to any one of Claims 12 to 15, characterized in that in at least one of the step (a) and step (b), at least one of oxygen, hydrogen and sulfur is added to relieve strain in the AlN layer resulting from lattice mismatch with the semiconductor substrate.

[Claim 17] The method for forming a film according to any one of Claims 12 to 15, characterized in that, by using a semiconductor substrate of which the principal plane is tilted against the (100) plane in a direction to expand lattice mismatch of the substrate with the AlN layer, the dielectric constant of the AlN layer increases.

[Claim 18] A method for forming a film, characterized by comprising a step (a) of exposing a surface of a semiconductor substrate to an atmosphere including one of nitrogen, hydrogen, sulfur and magnesium to terminate dangling bonds on the surface of the semiconductor substrate, and a step (b) of forming a crystalline AlN layer on the semiconductor substrate.

[Claim 19] The method for forming a film according to Claim 18, characterized in that:

before the step (b), the step of nitrogenizing the surface of the semiconductor substrate to form a silicon nitride layer is further included; and

in the step (b) a crystalline AlN layer is formed on the silicon nitride layer.

[Claim 20] The method for forming a film according to Claim 18 or 19, characterized in that, in the step (b), at least one of oxygen, hydrogen and sulfur is added to the AlN film to relieve strain in the AlN layer resulting from lattice mismatch with the semiconductor substrate.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a method for forming a film which comprises a high-resistance group-III-V dielectric crystal including aluminum (Al) and nitrogen (N), and a semiconductor element using the same.

[Prior Art]

In recent years, considerable progress has been made in CMOS devices formed on Si substrates with regard to the miniaturization of the elements constituting these devices, such as MOS transistors, and the high integration of these elements. Along with these advancements in miniaturization and high integration, a strong demand has developed for an improvement in the capacitance per unit area of the gate insulating film, which is an element of an MOS transistor, for example, so as to reduce the power source voltage for operating the elements of an MOS device in order to conserve power. However, to ensure the charge that is necessary to perform the same element operation as has been conventionally done, the capacitance per unit area of the gate insulating film must be raised.

Broadly speaking, there are two methods for increasing the capacitance of the gate insulating film. The first method is to make the gate insulating film thin, and the second method is to make the gate insulating film of a material with a higher dielectric constant. That is to say, there are two approaches to improving the performance of the gate insulting film: making it thin and increasing the dielectric constant.

As for the thinning of the gate insulating film, a particularly large number of attempts to achieve it have been made by performing thermal oxidation of an Si substrate with higher precision. The method of fabricating a silicon dioxide (SiO_2) insulating film by thermal oxidation of the Si substrate is advantageous in that with this method, for example, the formation of an oxide film is easy, the oxide film has extremely good properties as a gate insulating film, including a low interface state density, high breakthrough voltage properties, and small current leakage, and moreover the fabrication process of the oxide film can sufficiently adapt to the miniaturization and high integration

of elements. Therefore, with regard to the current CMOS transistors that are formed on Si substrates, it would not be an overstatement to say that apart from thermal oxidation, there are no other methods in practical use for the manufacture of gate insulating films. Consequently, most studies on increasing the performance of gate insulating film properties address how to make the SiO_2 films thinner. For example, as disclosed in "THE NATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (THE SEMICONDUCTOR INDUSTRY ASSOSIATION in the U.S.A) page 74, table 22" (first document), which assesses future perspectives for Si transistor research, it is predicted that the thickness of gate insulating films, which in the year 1997 was 4 to 5 nm, will become 2 to 3 nm by the year 2001. Moreover, as a study of how to meet the demands for thinner SiO_2 films, the "TECHNICAL REPORT OF IEICE, ED98-9, SDM98-9 (1998-04) page 15" (second document) discloses a method for thermal oxidation using a fast oxidation process with rapid-heating and rapid-quenching. According to the method in this document, the film thickness of the fabricated SiO_2 film is 1.5 nm.

An example of a method for increasing the dielectric constant of the material that forms the gate insulating film is disclosed in "APPLIED PHYSICS LETTERS 72, 2835, (1998)" (third document). This method uses a layered film of $SiO_2/Ta_2O_5/SiO_2$ (three-layer film) as the gate insulating film instead of using only an SiO_2 single layer film. By utilizing this layered state having the large relative dielectric constant of the Ta_2O_5 of 20 to 25, the amount of stored charge per unit area is raised. Simultaneously, extremely thin SiO_2 layers, which are formed by direct thermal oxidation of the Si, are interposed between the Ta_2O_5 and the Si substrate to avoid introducing a high density of interface states to the interface between the Si substrate and the insulating film made of a high dielectric material when the insulating film is in contact with the Si substrate.

From a requirement separate from those mentioned above, attempts have been made to make gate insulating films with materials other than SiO_2. For example, in the method disclosed in JP H01-64789A (fourth document), the gate insulating film is made

using Yttrium Stabilized Cubic Zirconia (hereinafter, abbreviated as YSZ) instead of SiO_2, so as to be increased in the breakthrough properties of the gate insulating film when it is irradiated with high energy radiation by X-ray exposure, for example. In contrast to the normally amorphous SiO_2 and Ta_2O_5, the YSZ used here has crystallinity.

From further separate requirements, there have been attempts to make the gate insulating film with a material other than SiO_2. For example, in the method disclosed in "JAPAN JOURNAL OF APPLIED PHYSICS 35, 4987 (1996)" (fifth document), studies were conducted for attaining a transistor with memory effect using a thin film with ferroelectric properties as the gate insulating film of a field effect transistor. Here a $PbZr_{1-x}Ti_xO_3$ (PZT) thin film, which has particularly good ferroelectric properties, was used as the gate insulating film. However, this PZT film is hard to form directly onto an Si substrate, so an insulating film made of a different material like CeO_2 was interposed between the PZT film and the Si substrate.

[Problems that the Invention is to solve]

However, there are several problems with making SiO_2 films thin and developing new gate insulating film materials as in the above-mentioned documents, as will be shown in the following.

The first document predicts that by the year 2006 a gate film thickness of 1.5 to 2 nm will be achieved, but does not expected that it is possible to achieve an SIO_2 film at a thickness thinner than 1.5 nm beyond that point. Moreover, it presents no further solutions. That is, it is believed that reducing the thickness of an SiO_2 film to 1.5 nm or less and using that film as the gate insulating film of a device is unachievable. It would appear that the reason for this is that, in an SiO_2 film thinner than 1.5 nm, a direct tunneling current flows through the film. This occurrence of a direct tunneling current is a particularly serious problem in the memory cell transistors of DRAMs. Thus, there is a demand for a new gate insulating film material with a higher dielectric constant and properties (like a low density of interface states) on a par with SiO_2 films, so as to secure a

desired charge using a film of a thickness at which direct tunneling current does not occur.

The second document reports that an extremely thin SiO_2 film of 1.5 nm has been fabricated which are excellent in properties, such as breakdown voltage, leakage properties, and high frequency properties. On the other hand, it has very serious deficiencies with regard to its reliability. That is, there is a notable occurrence of impurity (boron, for example) penetration from the gate electrode when a very thin SiO_2 film is used as a gate insulating film. For example, the second document reports that when a gate electrode made of polycrystalline silicon was provided on the gate insulating film in a PMOSFET, how the boron (B) used as a dopant passed from the gate electrode through the SiO_2 film and penetrated into the Si substrate.

The third document reports that with a three-layered film structure introduced to attain increased breakthrough voltage, the equivalent thickness of the film to the SiO_2 can be given at 2.3 nm. However, the interface state density was three times that of an SiO_2 film with a film thickness of 2.3 nm.

In the fourth document, a gate insulating film made of YSZ was fabricated, but since YSZ tends to pass molecules and ions through itself easily enough that it is used in oxygen sensors for automobile engines, current leakage easily occurs between the gate electrode and the channel due to the contribution of ionic conduction, for example. This means that it is difficult to obtain, using YSZ, a gate insulting film having a high breakthrough voltage and reliability.

In the fifth document, a buffer layer made of a CeO_2 film must be fabricated before the PZT film, which is a ferroelectric film, is formed. Since ferroelectric materials other than PZT often include heavy metals such as Bi, Pb, Ta, Sr or Ba, there is a large risk that these metals will diffuse into the Si substrate and negatively affect the electrical characteristics of the channel. The results of the secondary ion mass spectrometry (SIMS) measurements in this document indicate that Pb had diffused into the Si substrate. Additionally, as these ferroelectric materials are oxides of composite materials, there is a

large risk that an SiO_2 region will be formed at the interface between the ferroelectric film and the Si substrate. When an SiO_2 region is formed at this interface, there is the problem that a large part of the voltage applied to the gate electrode in the MOS transistor structure often gets applied to this low dielectric constant SiO_2 region, thereby lowering the effective voltage applied to the ferroelectric film itself. Thus, there is the problem that switching of the transistor is not carried out efficiently.

Thus, an object of the present invention is to provide a method for fabricating a film which can sufficiently keep up with progress in the miniaturization and high integration of elements, and a semiconductor element which uses the same, by using a material for the gate insulating film material which is different from the gate insulating film materials that have already been disclosed above and with which superior properties can be attained.

[Means for Solving the Problems]

A semiconductor element according to the present invention includes an insulating film and a conductor electrode on a semiconductor substrate, and the insulating film is at least partially formed of an AlN layer.

Thus, there is an increase in the capacitance per unit area of the entire insulating film having an AlN layer with a higher dielectric constant than a silicon oxide film fabricated by thermal oxidation. Further, in the compact crystalline AlN layer, there are hardly any defects or interface states, so the AlN layer can achieve good reliability on par with the silicon oxide film. Also, this insulating film can be used as a gate insulating film of a field effect transistor or a capacity insulating film of an MIS capacitor.

When the semiconductor element is a field effect transistor, the insulating film functions as a gate insulating film of the field effect transistor.

In the semiconductor element, the AlN layer is preferably a single crystal layer epitaxially grown on the substrate.

In the semiconductor element, when the plane direction of principal plane of the

semiconductor substrate is the (100) plane, then the AlN can be a cubic crystal of which principal plane is the (100) plane.

In the semiconductor element, since the semiconductor substrate is formed of Si, a high crystalline AlN layer can be obtained by making use of the resemblance in crystal structure between AlN and Si.

In the semiconductor element, by terminating the dangling bonds at the surface of the semiconductor substrate by any one of aluminum, nitrogen, hydrogen, sulfur and magnesium, the density of the interface states at the interface of the insulating film with the semiconductor substrate can be reduced.

In the semiconductor element, by further providing the insulating film with a silicon nitride layer interposed between the AlN layer and the semiconductor substrate, it is possible to maintain the crystallinity of a base, the Si substrate, as it is, while due to the presence of the silicon nitride layer, further reducing the dangling bonds at the surface of the semiconductor substrate, and significantly reducing the density of the interface states at the interface of the insulating film with the semiconductor substrate. Also, with the silicon nitride layer, it is also possible to prevent impurities from passing through the AlN layer and diffusing to the semiconductor substrate.

By further providing the insulating film with a dielectric layer which is formed on the AlN layer and which is made of at least one of a dielectric material with a higher dielectric constant than AlN, and a material having ferroelectric properties, the semiconductor element, which is given the structure of a field effect transistor, can function as an MFISFET, for example. In this case, by providing a dielectric layer on the highly crystalline AlN layer, a highly crystalline tetragonal dielectric layer can be attained. Consequently, it is possible to attain a high dielectric film with a higher dielectric constant or a ferroelectric film with even better remanence retention properties.

When a dielectric layer is further provided to the insulating layer, wherein the dielectric layer is formed on the AlN layer and made of at least one of a dielectric material

with a higher dielectric constant than the AlN, and a material having ferroelectric properties, and a crystalline conductive element is provided at least either above or below the dielectric layer, the semiconductor element can function as an MFMISFET, for example.

In the semiconductor element, by including at least one of oxygen, hydrogen and sulfur in the AlN layer to relieve strain in the AlN layer resulting from lattice mismatching with the semiconductor substrate, a highly reliable semiconductor element with a gate insulating film that only slightly deteriorates over time can be achieved.

In the semiconductor element, it is also possible to expand lattice mismatching of the AlN layer with the semiconductor substrate so as to be increased in the dielectric constant of the AlN layer.

A first method for forming a film according to the present invention includes alternately repeating a step (a) of forming either one atom layer of an Al atom layer and an N atom layer on a semiconductor substrate of which a plane orientation of the principal plane is the (100) plane, and a step (b) of forming the other atom layer of the Al atom layer and the N atom layer on said one atom layer, thereby forming an AlN layer which is a cubic crystal having the (100) plane.

With this method, a high crystalline AlN layer is formed on a (100) substrate generally used. Although an AlN layer having a hexagonal and wurtzite type crystal structure, which is the original structure of AlN, is formed on a (111) substrate, it is difficult for the (111) substrate to be mass-produced due to its high cost. On the other hand, with the (100) substrate generally used, AlN, which would originally have a hexagonal and wurtzite type crystal structure, can grow successively on a diamond-crystal-structure Si substrate in the form of cubic and Zinc blende crystal. Accordingly, this method can be made available for fabricating a field effect transistor with a high crystalline AlN layer used as a gate insulating film and a capacitor with an AlN film used as a capacity insulating film.

In the first method for forming a film, deposition of the Al atom layer and the N atom layer is preferably performed by a molecular beam epitaxy (MBE) method or metal organic vapor phase epitaxy (MOVPE) method.

In the first method for forming a film, an Si substrate is preferably used as the semiconductor substrate.

In the first method for forming a film, if the step of nitrogenizing the surface of the semiconductor substrate to form a silicon nitride layer is further included before the step (a), and said one atom layer is formed on the silicon nitride layer in the step (b), then the dangling bonds at the surface of the semiconductor substrate can be further reduced.

In the first method for forming a film, in at least one of the step (a) and step (b), at least one of oxygen, hydrogen and sulfur is added to relieve strain in the AlN layer resulting from lattice mismatch with the semiconductor substrate. Further, by using a semiconductor substrate of which the principal plane is tilted against the (100) plane so that lattice mismatch with the AlN layer is expanded, the dielectric constant of the AlN layer can increase.

A second method for forming a film according to the present invention includes a step (a) of exposing a surface of a semiconductor substrate to an atmosphere including one of nitrogen, hydrogen, sulfur and magnesium to terminate dangling bonds on the surface of the semiconductor substrate, and a step (b) of forming a crystalline AlN layer on the semiconductor substrate.

With this method, since the AlN layer is formed in a state wherein the dangling bonds on the surface of the semiconductor substrate have been terminated, an AlN film with a small interface state density and excellent non-deterioration properties, for example, can be obtained.

In the second method for forming a film, if the step of nitrogenizing the surface of the semiconductor substrate to form a silicon nitride layer is further included before the step (b), and a crystalline AlN layer is formed on the silicon nitride layer in the step (b),

then the dangling bonds at the surface of the semiconductor substrate can be terminated even more reliably.

In the second method for forming a film, it is preferable that in the step (b) at least one of oxygen, hydrogen and sulfur is added to the AlN film to relieve strain in the AlN layer resulting from lattice mismatch with the semiconductor substrate.

[Embodiments of the Invention]

- Regarding the Basic Characteristics of AlN -

Before the embodiments of the present invention are described, first a description will be given regarding the basic characteristics of the AlN film used in the present invention as a new material for gate insulating films, for example.

Fig. 7 is a band diagram for comparing the band discontinuities of the energy bands of AlN and SiO_2 with respect to Si.

As shown in Fig. 7, the band gap of SiO_2 (difference in energy level between conduction band and valance band; in other words, the width of the forbidden zone) is approximately 9 eV. There is a band discontinuity of approximately –4.7 eV between the valance band edge of SiO_2 and the valance band edge of Si. Moreover, there is a band discontinuity of approximately 3.2 eV between the conduction band edge of SiO_2 and the conduction band edge of Si. On the other hand, the band gap of AlN is approximately 6.4 eV. There is a band discontinuity of approximately –3.0 eV between the valance band edge of AlN and the valance band edge of Si. Moreover, there is a band discontinuity of approximately 2.1 eV between the conduction band edge of AlN and the conduction band edge of Si. This means that the band discontinuity between AlN and Si is 64% (valance band side) and 66% (conduction band side) of the band discontinuity between SiO_2 and Si.

Moreover, as there is only a very small number of impurities or defects generating carriers in the AlN film, high insulation properties thereof can be maintained. Also, AlN has few Si dangling bonds at the interface with Si, so there is an extremely low interface state density thereof at the interface with Si.

These facts show that AlN films can be adequately used as gate insulating films or other barrier layers by interposing the AlN film between the Si and the conductor in opposition to the Si.

Silicon crystals have a diamond structure, and AlN crystals have a wurtzite type crystal structure resembling the crystal structure of zinc blende. Zinc blende crystal structures are a type of cubic, in which one type of atoms in a diamond type structure are replaced with a different type of atoms at every other atom, and therefore it is easy to epitaxially grow zinc blende type crystals on diamond type crystals. On the other hand, it is normally difficult to epitaxially grow wurtzite type crystals, which are a type of hexagonal crystals, on diamond type crystals. However, in their (111) plane, wurtzite type crystal structures and zinc blende type crystal structures have the same atom arrangement. This means that a hexagonal, wurtzite type AlN layer can be epitaxially grown on an Si substrate in which the (111) plane is the principal plane of the Si substrate (hereinafter, referred to as the (111) Si substrate). This is a conventionally known fact.

Here, the inventor first noted that if the AlN crystal is sufficiently thin, a (100) AlN layer with a hexagonal, zinc blende type crystal structure is formed on an Si substrate in which the (100) plane is the principal plane (hereinafter, referred to as the (100) Si substrate). The AlN layer is of course highly crystalline in its original wurtzite type crystal form, but also in a zinc blende type crystal form.

Then, by suitably choosing the AlN growth conditions and the plane orientation of the Si substrate, a highly crystalline AlN film can be epitaxially grown on a single crystal silicon layer.

On the other hand, the relative dielectric constant of AlN is 9, which is significantly larger than the relative dielectric constant of 3.9 of SiO_2 formed by thermal oxidation. Thus, using AlN as the material for the gate insulating film, for example, makes it possible to significantly improve the capacitance per unit area, and it is unnecessary to make the AlN film as thin as an SiO_2 film for obtaining the same

capacitance as an SiO_2 film. That is, the amount of stored electric charges can be improved while direct tunnel leakage of the carriers is suppressed. Thus, AlN films can sufficiently keep up with advancements in the miniaturization and high integration of semiconductor elements.

As documents addressing the fabrication of a group-III nitride crystalline thin film on an Si substrate, there is a sixth document "T. Lei and T. D. Moustakas, J. Appl. Phys. 71, 4934, (1992)", and a seventh document "A. Watanabe, T. Takeuchi, K. Hirosawa, H. Amano, K. Hiramatsu, and I. Akasaki, J. Crystal Growth 128, 391, (1993)."

However, in both documents the AlN film is used as a buffer layer before the formation of a GaN layer, and no attempts of using the AlN film as an element component, such as a gate insulating film, are to be found.

(FIRST EMBODIMENT)

In a first embodiment of the present invention, a method for fabricating a basic AlN film by molecular beam epitaxy (MBE) using a molecular beam epitaxy device is described. Figs. **1(a)** to **1(d)** are cross sectional views illustrating the procedure for forming an AlN film according to the first embodiment.

As explained later, it is also possible to form an AlN insulating film on an Si substrate using a device other than the MBE device.

First, in the process shown in Fig. **1(a)**, after the cleaning of an Si substrate **1** for the fabrication of an element, the Si substrate **1** is soaked in a liquid including hydrogen fluoride (HF) or ammonium fluoride (NH_4F), rinsed with water and dried, and then immediately introduced into an MBE device for growing crystals. At this time, the surface of the Si substrate is coated with hydrogen (H) atoms or an extremely thin SiO_2 amorphous layer. The principal plane of the Si substrate **1** is preferably the (100) plane, but it can also be the (111) plane or another higher-order plane, or a plane set several degrees off of those planes. In the MBE device, the Si substrate **1** is heated to a temperature in the range of 100 to 400°C, thereby removing moisture and/or adsorption

gas remaining on the surface of the Si substrate **1**.

Then, the temperature of the Si substrate **1** is raised further and maintained within the range of 800 to 900°C. At this time, the H atoms or the thin SiO_2 amorphous layer coating the surface of the Si substrate **1** are removed, thereby leaving behind dangling bonds **2**, as shown in Fig. **1(a)**.

Next, in the step shown in Fig. **1(d)**, with an MBE growth method, materials for forming Al atom layers and materials for forming N atom layers are supplied in alternation to alternately stack one by one single atom layers of Al atoms and N atoms, thus forming an AlN crystal layer **7** stacked with tens layers.

As this process moves from Fig. **1(a)** to Fig. **1(d)**, there are two types of structures that may be formed depending on the type of atoms at the interface region where the Si substrate **1** is bonded to the AlN crystal layer **7**.

As mentioned above, in either the (100) plane or the (111) plane of the AlN crystal layer **7**, planes formed only of Al atoms **3**, and planes formed only of N atoms **4**, appear alternately. Consequently, there is the case shown in Fig. **1(b)**, in which an interface region **5a** is formed in the AlN crystal layer **7** wherein the Si atoms at the surface of the Si substrate **1** are bonded to the Al atoms **3**, and there is the case shown in Fig. **1(c)**, in which an interface region **5b** is formed in the AlN crystal layer **7** wherein the Si atoms at the surface of the Si substrate **1** are bonded to the N atoms **4**. Which one of these states shown in Fig. **1(b)** and Fig. **(b)** occurs is determined by whether the Al atom layer forming materials are supplied first or the N atom layer forming materials are supplied first during the MBE growth.

The properties of the AlN crystal layer **7** when the AlN crystal layer **7** has the interface region **5a** shown in Fig. **1(b)** are not totally equivalent to those of the AlN crystal layer **7** and when it has the interface region **5b** shown in Fig. **1(c)**, but both cases are similar in that the fabricated AlN crystal layer **7** has a structure with good crystallinity.

However, because it is undesirable that Al atoms acting as p-type impurities

migrate into the Si substrate **1**, it is often the case that the state shown in Fig. **1(c)** is the preferable of the two. That is, it is safe to say that it is mostly preferable to first supply the material gas for forming N atom layers.

(SECOND EMBODIMENT)

In a second embodiment, a separate example of a method for forming a basic AlN film by molecular beam epitaxy (MBE) using a molecular beam epitaxy device is described. Figs. **2(a)** to **2(g)** are cross sectional views illustrating the procedure for forming an AlN film according to the present embodiment.

First, like in the first process according to the first embodiment, after the cleaning of the Si substrate **1** for the fabrication of an element, the Si substrate **1** is soaked in a liquid including hydrogen fluoride (HF) or ammonium fluoride (NH_4F), rinsed with water and dried, and then immediately introduced into an MBE device for growing crystals. At this time, the surface of the Si substrate is coated with hydrogen (H) atoms or an extremely thin SiO_2 amorphous layer. The principal plane of the Si substrate **1** is preferably the (100) plane, but it can also be the (111) plane or another higher-order plane, or a plane set several degrees off of those planes. In the MBE device, the Si substrate **1** is heated to the range of 100 to 400°C, thereby removing moisture and/or adsorption gas remaining on the surface of the Si substrate **1**.

In the first embodiment, this was followed by further raising the temperature of the Si substrate **1** and maintaining it at a temperature in the range of 800 to 900°C, thereby leaving dangling bonds on the Si substrate, and then the AlN crystal layer was formed on those dangling bonds. However, in the present embodiment the termination atoms are left on the surface of the Si substrate **1**, and the AlN crystal layer is formed on those termination atoms.

As shown in Fig. **2(a)**, when the surface of the Si substrate **1** is covered with hydrogen atoms **10**, this is followed by stopping the rise in temperature of the substrate near 500°C.

Then, as shown in Fig. **2(d)**, the hydrogen atoms **10** are left remaining as the termination atoms **12** of the dangling bonds.

On the other hand, when the surface of the Si substrate **1** is covered with an SiO_2 amorphous layer, or other chemical species or thin layer, the Si substrate **1** is further maintained within a temperature range of 800 to 900°C. At this time, the other chemical species or thin SiO_2 amorphous layer serving as the surface covering is removed from the surface of the Si substrate **1**. Then, as shown in Fig. **2(b)**, dangling bonds **2** are left behind on the surface of the Si substrate **1**. Next, as shown in Fig. **2(c)**, termination chemical species **11** are supplied to the dangling bonds **2** on the Si substrate **1**.

As shown in Fig. **2(d)**, the result is that the chemical species **11** are kept as the termination atoms **12** and that the dangling bonds **2** are terminated. For the termination chemical species **11** used at this time, one can be chosen from the group consisting of hydrogen (H), Mg, sulfur (S), nitrogen (N) or aluminum (Al), for example.

Then, as mentioned above, in either case AlN is epitaxially grown after the dangling bonds on the surface of the Si substrate **1** are terminated by the termination atoms.

Then the AlN crystal layer **7** is formed in the step shown in Fig. **2(g)**. Here, as the process moves from Fig. **2(d)** to Fig. **2(g)**, whether the atoms at the bottom end of the interface region of the AlN crystal layer **7** are Al or N is determined, as explained in the first embodiment, by which type of material gas is supplied first during the MBE growth, but whether it is easier for the Al atoms **3** or for the N atoms **4** to attach to this bottom end may depend on the type of termination atoms **12** on the surface of the Si substrate **1**.

Then, in either the (100) plane or the (111) plane of the AlN crystal layer **7**, planes formed only of Al atoms **3**, and planes formed only of N atoms **4**, appear in alternation. Consequently, there is the case shown in Fig. **2(e)**, in which an interface region **5a** is formed wherein in the AlN crystal layer **7** the termination atoms **12** at the surface of the Si substrate **1** are bonded to the Al atoms **3**, and there is the case shown in Fig. **2(f)**, in which an interface region **5b** is formed wherein in the AlN crystal layer **7** the termination atoms

12 at the surface of the Si substrate 1 are bonded to the N atoms 4. The properties of the AlN crystal layer 7 when it has the interface region 5a shown in Fig. 2(e), and when it has the interface region 5b shown in Fig. 2(f), are not completely equivalent, but in both cases the AlN crystal layer 7 has a structure with good crystallinity.

However, also in the present embodiment, because it is undesirable for Al atoms, which act as p-type impurities, to migrate into the Si substrate 1, it is often the case that the state shown in Fig. 2(f) is more preferable. That is, one could say that it is mostly preferable to first supply the material for forming the N atom layers.

According to the method of the present embodiment, in the step shown in Fig. 2(d), the AlN crystal is grown after the dangling bonds on the surface of the Si substrate 1 have been terminated by the termination atoms 12. Therefore, in comparison to the method of the first embodiment, there is the benefit that the density of the interface states in the formed AlN crystal layer 7 can be more reliably reduced.

Moreover, in the present embodiment, since a single atom layer made of termination atoms 12 is interposed between the AlN crystal layer 5 and the Si substrate 1, so there is the advantage that suitably selecting the chemical species for forming the termination atoms 12 makes it possible to more effectively suppress the migration of Al atoms into the Si substrate 1.

(THIRD EMBODIMENT)

A third embodiment describes a method for forming a layered film when a layered structure in which a separate crystal layer is layered on the AlN crystal layer is used as the gate insulating film of a 3 terminal- or 4 terminal-type field effect transistor functioning as a MFISFET, for example. Figs. 3(a) to 3(c) are cross sectional views showing the process steps for forming a layered film having an AlN film and a dielectric thin film according to the third embodiment.

First, in the steps shown in Figs. 3(a) and 3(b), the fabrication process according to either of the above-mentioned first or second embodiments is used to form the AlN crystal

layer 7 on the Si substrate **1**.

Then, in the step shown in Fig. **3(c)**, a dielectric thin film **8** having crystallinity is formed on the AlN crystal layer 7. It is preferable that for the dielectric material constituting the dielectric thin film **8**, a material is used that has a relative dielectric constant (ε r) that is at least larger than the relative dielectric constant of 3.9 of a directly oxidized SiO_2 film. A polysilicon film **9** for the gate electrode is then formed on the dielectric thin film **8**.

The material for forming the dielectric thin film **8** preferably has high crystallinity, but can also be amorphous. To fabricate the dielectric thin film **8** having high crystallinity, in the case of the (111) Si substrate, the (0001) plane of a hexagonal structure (wurtzite-type structure) matches the (111) plane of the Si substrate. Therefore, it is preferable to use a dielectric material with a hexagonal structure. Additionally, in the case of the (100) Si substrate, the (100) plane of a cubic structure (zinc blende type structure) matches the (100) plane of the Si substrate. Therefore, it is preferable to use a dielectric material with a cubic structure. However, if the dielectric thin film is extremely thin, it is possible to hold the crystal structure of the Si substrate **1** as is, and hence there is no limitation to the above configurations of crystal structure.

Furthermore, when the dielectric thin film **8** has crystallinity, it is preferable that the lattice constant thereof is close to the lattice constant of the AlN crystal layer 7 or the lattice constant of the Si substrate **1**. More specifically, CeO_2, which has a lattice mismatch percentage of –0.37% with Si, ZrO_2, which has a lattice mismatch percentage of –5.4% with Si, or a crystal mixture thereof, for example, are conceivable as examples of a dielectric material for forming the dielectric thin film **8**.

The dielectric material for forming the dielectric thin film **8** can also be MgO, for example, which has a lattice mismatch percentage of –4.5% with AlN.

By using a material such as the above to form the dielectric material **8**, the relative dielectric constant (ε r) of the entire layered structure of the AlN crystal layer 7 and the

dielectric thin film **8** together can be set at two or more times as high as the dielectric constant of an SiO_2 film. This means that the entire layered structure of the AlN crystal layer 7 and the dielectric thin film **8** together can be used as the gate insulating film to achieve a gate insulating film having a high capacitance per unit area.

It is also possible to use a crystalline thin film having not only a large dielectric constant but also ferroelectric properties for the dielectric thin film **8**. In this case, examples of ferroelectric material include barium titanate ($BaTiO_3$), PZT ($PbZrO_3$-$PbTiO_3$), and PLZT (oxide including Pb, La, Zr, and Ti). Here, by forming a ferroelectric material on the highly crystalline AlN crystal layer 7, the crystallinity of the dielectric thin film **8** having ferroelectric properties can be made significantly higher than when the dielectric thin film **8** is formed on a thin film having an amorphous structure. The result is that the dielectric constant of the dielectric thin film **8** with high crystallinity and ferroelectric properties can be markedly increased, and the relative dielectric constant (ε r) of the entire layered structure including the AlN crystal layer 7 and the dielectric thin film **8** becomes significantly high.

At this time the highly crystalline AlN crystal layer 7 functions as a buffer layer when the dielectric thin film **8**, which either has a higher dielectric constant than AlN or has ferroelectric properties, is layered onto the Si substrate **1**.

Then, because the AlN crystal layer 7 has a high crystallinity and is compact, the diffusion of impurities from the dielectric thin film **8**, which is made of a highly dielectric material or a ferroelectric material that includes heavy metals, for example, can be suppressed. Also, because the AlN crystal layer 7 itself has a high dielectric constant, the proportion of the voltage applied to the gate electrode that gets applied to the AlN crystal layer 7 functioning as a buffer layer can be reduced to less than one half of the voltage when an SiO_2 film is used as a buffer layer.

Also, because the AlN crystal layer 7 has high crystallinity, the dielectric thin film **8** formed on the AlN crystal layer 7 is highly orientated or crystallized reflecting the

crystallinity of the AlN crystal layer 7, and thus an even higher dielectric constant of the film can be achieved, or more stable remanence retention properties of the film can be obtained.

(FOURTH EMBODIMENT)

A fourth embodiment describes a method for forming a layered film when a layered structure, in which separate crystal layers are layered above and below the AlN crystal layer, is used as the gate insulating film of a 3 terminal- or 4 terminal-type field effect transistor functioning as a MFMISFET, for example. Figs. **4(a)** to **4(e)** are cross sectional views showing the steps for forming the layered film according to the fourth embodiment, which includes an AlN crystal layer, a crystalline dielectric thin film, a conductive thin film, and a ferroelectric film.

First, in the process steps shown in Figs. **4(a)** and **4(b)**, the fabrication process of either of the above-mentioned first or second embodiments is used to form the AlN crystal layer 7 on the Si substrate **1**.

Next, in the process step shown in Fig. **4(c)**, a first conductive thin film **21** having crystallinity is formed on the AlN crystal layer 7. $CoSi_2$, for example, is a possible material for forming the crystalline, first conductive film **21**.

Then, in the process step shown in Fig. **4(d)**, a crystalline dielectric thin film **22** made of a highly dielectric or ferroelectric material is formed on the first conductive thin film **21**. Possible materials for forming the crystalline dielectric thin film **22** include barium titanate ($BaTiO_3$), PZT ($PbZrO_3$-$PbTiO_3$), and PLZT (oxide including Pb, La, Zr, and Ti), for example.

Next, in the process step shown in Fig. **4(e)**, a second conductive thin film **23** is formed on the crystalline dielectric thin film **22**. $CoSi_2$, for example, is a possible material for forming the crystalline, second conductive film **23**.

The first conductive thin film **21** and the second conductive thin film **23** here are provided above and below the crystalline dielectric thin film **22**, but it is also possible to

provide only the upper or lower of the conductive thin film.

By patterning the layered film of the present embodiment to form a gate structure and source and drain regions, the crystalline dielectric thin film **22** can be made to function as the floating gate electrode of a nonvolatile semiconductor memory device. Then, the charges stored in the crystalline dielectric thin film **22** can be moved to the first conductive thin film **21** or the second conductive thin film **23**, or between both, to erase or write data.

(FIFTH EMBODIMENT)

A fifth embodiment describes a method for forming a layered film when a layered structure, in which a separate amorphous layer is layered on the AlN crystal layer, is used as the gate insulating film of a 3 terminal- or 4 terminal-type field effect transistor functioning as a MFISFET, for example. Figs. **5(a)** to **5(c)** are cross sectional views showing the process steps for forming the layered film including the AlN film and an amorphous layer according to the fifth embodiment.

First, in the process step shown in Fig. **5(a)**, after the cleaning of an Si substrate **1** for the fabrication of an element, the Si substrate **1** is soaked in a liquid including hydrogen fluoride (HF) or ammonium fluoride (NH_4F), rinsed with water and dried, and then immediately introduced into a device for conducting nitrogenation and MBE growth. At this time, the surface of the Si substrate is coated with hydrogen (H) atoms or an extremely thin SiO_2 amorphous layer. The principal plane of the Si substrate **1** is preferably the (100) plane. However, it can also be the (111) plane or another higher-order plane, or a plane set several degrees off of those planes. In the device, the Si substrate **1** is heated to a temperature in the range of 100 to 400°C, thereby removing moisture and/or adsorption gas remaining on the surface of the Si substrate **1**.

Then, the temperature of the Si substrate **1** is raised further and maintained within the range of 800 to 900°C. At this time, the H atoms or the thin SiO_2 amorphous layer coating the surface of the Si substrate **1** is removed.

Next, in the step shown in Fig. **5(b)**, dried NH_3 gas or N_2O gas, or radical activated

nitrogen gas, is supplied to the Si substrate **1** to nitrogenize the Si on the surface of the Si substrate **1**, thereby forming a non-crystalline silicon nitride layer **25** made of a silicon nitride compound such as Si_3N_4. In this case the clean, smooth Si substrate surface is either irradiated with excited species of nitrogen molecules or atoms which are generated by high-frequency cells or helicon plasma cells, or irradiated with ammonia, or derivative molecules or ions thereof which are activated by applying extreme heat, to directly nitrogenize the Si. It is preferable that the silicon nitride layer **25** has an extremely small thickness of only a single molecule to several molecules, and is non-amorphous, and that its highly periodic properties are maintained.

Then, in the process step shown in Fig. **5(c)**, a crystalline AlN thin film **26** is layered by MBE growth method. At this time, although the silicon nitride layer **25** serving as the base for the AlN thin film **26** is amorphous, the silicon nitride layer **25** is extremely thin and is formed not by depositing a new nitride film with CVD, for example, but nitriding the Si substrate **1.** Therefore, the silicon nitride layer **25** maintains the regularity of the crystal structure of the Si substrate **1**. For that reason, the AlN thin film **26** formed on the silicon nitride layer **25** is substantially epitaxially grown reflecting the crystal structure in the Si substrate **1**, and thus high crystallinity thereof can be achieved.

Next, due to the presence of the silicon nitride layer **25**, the dangling bonds at the surface of the Si substrate **1** are terminated by nitrogen, and the density of interface states becomes extremely small. This means that using this layered film of an AlN thin film **26** and a silicon nitride layer **25** as the gate insulating film of a field effect transistor achieves a gate insulating film that has a high dielectric constant and high breakthrough properties.

(SIXTH EMBODIMENT)

A sixth embodiment describes a method for relieving strain in the AlN film caused by lattice mismatch between the AlN film and the Si substrate. The present embodiment describes by applying the process steps according to the aforementioned first through fifth embodiments, and figures showing these process steps have been omitted.

In the present embodiment, as in the above-mentioned embodiments, after the cleaning of the Si substrate for the fabrication of an element, the Si substrate is soaked in a liquid including hydrogen fluoride (HF) or ammonium fluoride (NH_4F), rinsed with water and dried, and then immediately introduced into a MBE device for growing crystals. At this time, the surface of the Si substrate is coated with hydrogen (H) atoms or an extremely thin SiO_2 amorphous layer. The principal plane of the Si substrate is preferably the (100) plane. However, it can also be the (111) plane or another higher-order plane, or a plane set several degrees off of those planes. In the MBE device, the Si substrate is heated to remove moisture and/or adsorption gas remaining on the surface of the Si substrate **1**. Then, the temperature of the Si substrate is further raised and the H atoms or the thin SiO_2 amorphous layer coating the surface of the Si substrate **1** are removed.

Then, as described in the first through fifth embodiments, an AlN film is formed on the Si substrate either directly or via a thin nitride film. At this time, with the MBE growth described in the first through fifth embodiment, oxygen, hydrogen, or sulfur impurities for example, are continually added to the AlN crystal layer **7** (or the AlN thin film **26**). Oxygen or hydrogen is supplied from the gas valve or gas cell disposed in the MBE device. Here, the oxygen or the hydrogen molecules can be supplied as they are, or can be activated into high frequency treated radicals, ions, or atoms and then supplied in the activated state. Sulfur can be supplied using a normal K-cell, or it can be supplied in a cracked state using a valve cracking cell, for example.

The above added elements are added individually or as mixtures of two or more types of atoms. Furthermore, the added amount of these elements is the dopant level, which should be in the range of 1×10^{15} cm^{-3} to 1×10^{20} cm^{-3}.

When the AlN layer including the above additives is used as the gate insulating film for a variety of transistors, these additives do not contribute to current leakage, which is a cause of deteriorated electrical properties of the transistor, and do not deteriorate the insulating properties of the gate insulating film.

Also, adding impurities, particularly the above-mentioned impurities, to the AlN layer at the range or 1×10^{15} cm^{-3} to 1×10^{20} cm^{-3} can relieve strain in the AlN layer resulting from a lattice mismatch caused by the different lattice constants between the Si substrate and the AlN layer. The result is that the introduction of crystal defects in the AlN layer such as dislocations are suppressed, and the crystallinity of the AlN layer is improved. Because strain is relieved in this manner, the deterioration of properties that occurring over time and the advancement of deterioration due to heating processes can be suppressed. Accordingly, it is possible to improve the reliability of a semiconductor element in which an AlN layer forms the gate insulating film or a part of the gate insulating film.

Contrary to the above method for relieving strain in the AlN layer, it is also possible to increase the dielectric constant of the AlN layer by tilting the principal plane of the Si substrate against the (100) plane to increase the strain within the AlN layer.

(SEVENTH EMBODIMENT)

A seventh embodiment describes the structure of a field effect transistor, which is one type of semiconductor elements having a gate insulating film including the AlN layer (the AlN crystal layer **7**, the AlN thin film **26**, or the layered film of the AlN layer and another thin film) formed with the methods illustrated in the first, second, third, or fifth embodiments. Fig. **6** is a cross sectional view of a field effect transistor according to the seventh embodiment.

As shown in Fig. **6**, a LOCOS film **52**, which is an insulating film for separating elements, is formed on an Si substrate **51**. Then, a gate insulating film **53**, which is made of only the AlN layer or the AlN layer and another thin film; a gate electrode **54** made of a low resistant polysilicon layer **54a** and a silicide layer **45b**; and insulating side walls **55**, which are made of a silicon oxide film and formed on both lateral faces of the gate electrode **54**, are provided on the active region surrounded by the LOCOS film **52** of the Si substrate **51**. Furthermore, low concentration source/drain regions **56** (LDD region)

interposing the region (channel region) positioned directly below the gate insulating film **53**, and high concentration source/drain regions **57** formed at the outer side of the low concentration source/drain region **56**, are provided in the Si substrate **1**. The impurities in the low concentration source/drain regions **56** and the high concentration source/drain regions **57** are p-type impurities (such as boron) when the field effect transistor is of the p-channel type, and n-type impurities (such as arsenic or phosphorus) when the field effect transistor is of the n-channel type.

As mentioned above, by constituting the gate insulating film of a 3 terminal- or 4 terminal-type field effect transistor using a highly crystalline AlN layer (or layered film having an AlN layer and another thin film), it is possible to significantly improve the capacitance per unit area of the gate insulating film over that of an SiO_2 film that has been formed by thermal oxidation. Consequently, where both have the same capacitance, the gate insulating film having an AlN layer can be given a larger film thickness than that having an SiO_2 film, so that the former gate insulating film hardly causes a leakage due to direct tunneling of the carriers. Also, because AlN has a large band discontinuity and there are only very few impurities or defects in the AlN layer that generate carriers, the AlN layer can maintain good insulating properties.

Furthermore, due to the resemblance in crystal structure and the nearness of the lattice constants of AlN and Si, a crystalline AlN layer is grown on the crystalline Si substrate. Thus the occurrence of dangling bonds at the interface region with the Si substrate can be inhibited, and the density of the interface states can be kept equal to or below that of an SiO_2 film formed by direct oxidation.

(OTHER EMBODIMENT)

In the above embodiments, the AlN layer (AlN crystal layer **7** or AlN thin film **26**) was formed by MBE. However, it is also possible to form a crystalline AlN layer using chemical vaporization deposition (CVD), metal organic vapor phase epitaxy (MOVPE), hydride vapor phase epitaxy (HVPE), or sputtering, for example.

Also, in the above embodiments, the AlN layer was used as the gate insulating film of an MOS transistor, but the AlN layer can also be used as the capacity insulating film of an MIS capacitor or an MIM capacitor.

Furthermore, an AlN layer having good crystallinity can be grown not only on Si substrates but also on GaAs substrates.

[Effects of the Invention]

In a semiconductor element according to the present invention, since an insulating film and a conductor electrode are provided on a semiconductor substrate and the insulating film is at least partially formed of an AlN layer, the semiconductor element enables an increase in the capacitance per unit area of the entire insulating film by making use of a crystalline AlN layer which has hardly any defects or interface states and which has good reliability on a par with the silicon oxide film. Therefore, a semiconductor element which can keep up with progress in the miniaturization and high integration of elements can be provided.

In a first method for forming a film according to the present invention, by alternately forming Al atom layers and N atom layers one on another over a semiconductor substrate of which a plane orientation of the principal plane is the (100) plane, a cubic-crystal AlN layer with the (100) plane is formed. Therefore, by making use of a (100) substrate generally used, this method can mass-produce a field effect transistor with the AlN layer used as a gate insulating film and a capacitor with an AlN film used as a capacity insulating film.

In a second method for forming a film according to the present invention, after the termination of dangling bonds on the surface of a semiconductor substrate, a crystalline AlN layer is formed on the semiconductor substrate. Therefore, the method can provide an AlN film with a small interface state density and excellent non-deterioration properties, for example.

In a third method for forming a film according to the present invention, since a

high crystalline AlN with high dielectric constant is used as a gate insulating film in an MFISFET structure, the method can attain an MFISFET in which a ferroelectric film formed on the AlN layer has even better remanence retention properties.

[Brief Description of the Drawings]

[FIG. 1]

Cross sectional views illustrating the procedure for forming an AlN crystal layer according to a first embodiment.

[FIG. 2]

Cross sectional views illustrating the procedure for forming an AlN crystal layer according to a second embodiment.

[FIG. 3]

Cross sectional views illustrating the process steps for forming an AlN crystal layer, a dielectric thin film, and a gate polysilicon film for use in an MFISFET, for example, according to a third embodiment.

[FIG. 4]

Cross sectional views illustrating the process steps for forming an AlN crystal layer, a crystalline dielectric thin film, and first and second conductive thin films, for use in an MFMISFET, for example, according to a fourth embodiment.

[FIG. 5]

Cross sectional views illustrating the process steps for forming a silicon nitride layer, an AlN thin film, and a polysilicon film, for use in an MISFET, for example, according to a fifth embodiment.

[FIG. 6]

A cross sectional view showing the structure of an MISFET according to a seventh embodiment.

[FIG. 7]

A band diagram showing the energy bands of an Si crystal, an SiO_2 dielectric and

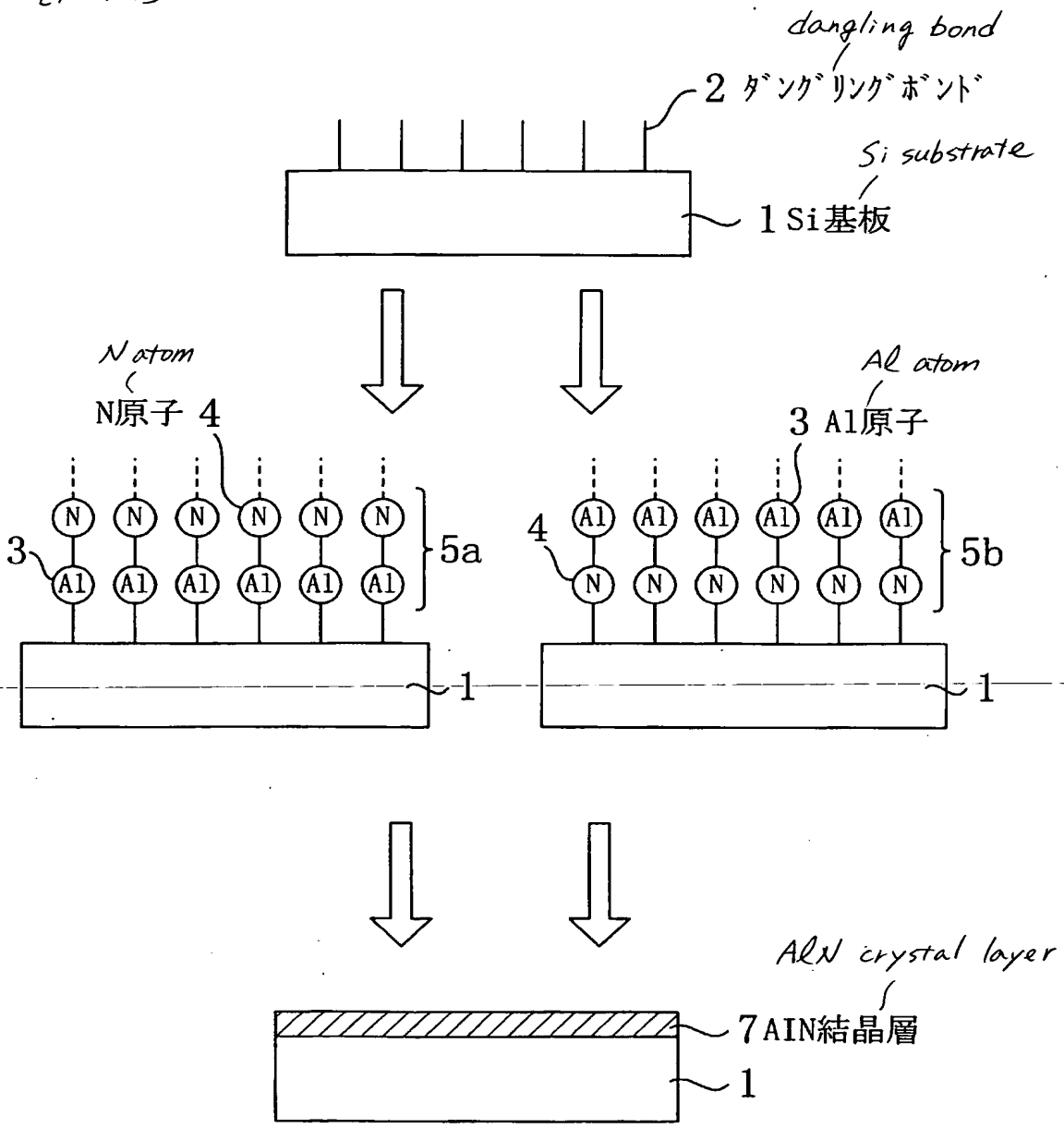
an AlN crystal.

[Explanation of the Reference Numerals]

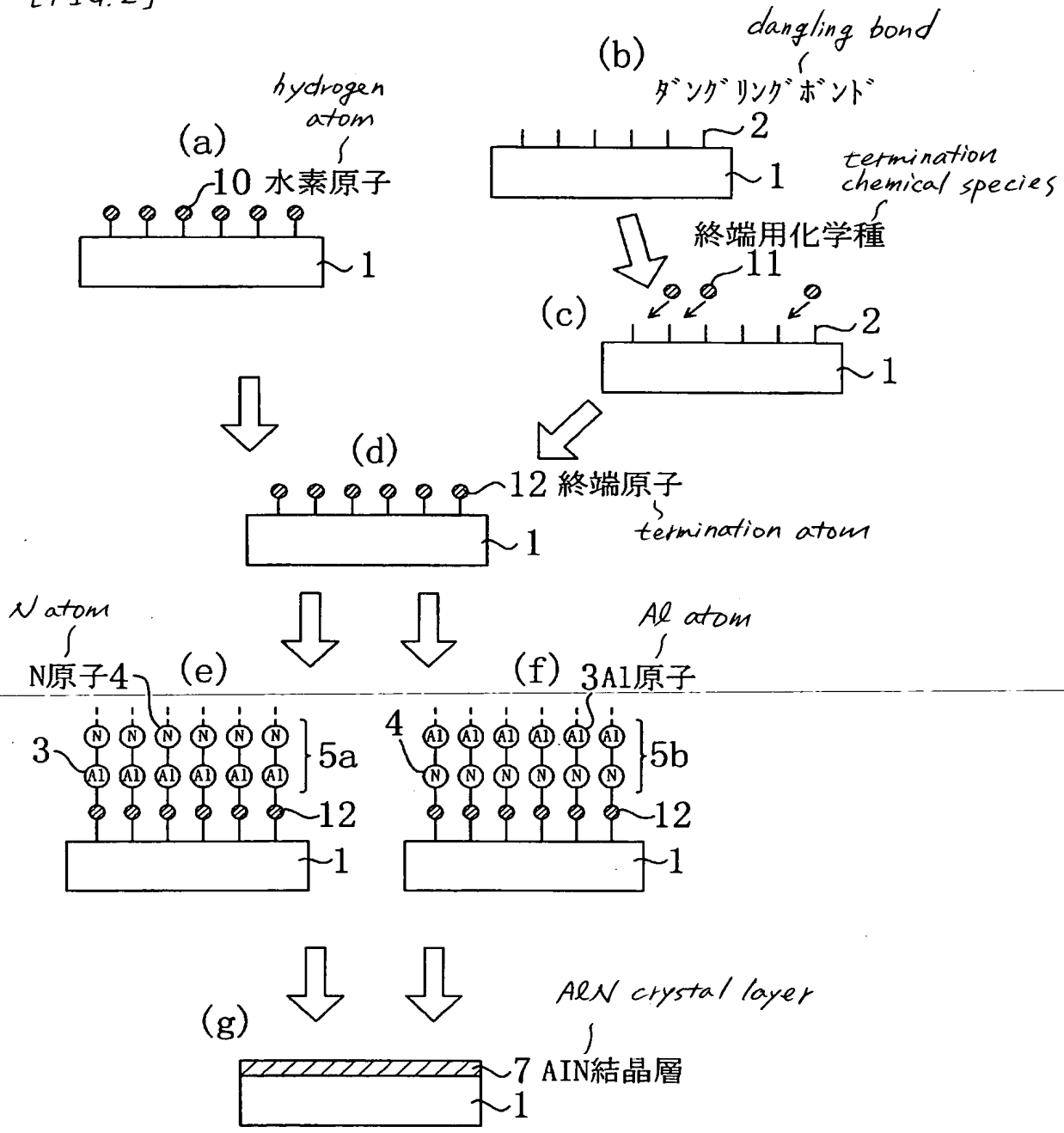
1	Si substrate
2	dangling bond
3	Al atom
4	N atom
5	interface region
7	AlN crystal layer
8	dielectric thin film
9	polysilicon film
10	hydrogen atom
11	termination chemical species
12	termination atom
21	first conductive thin film
22	crystalline dielectric thin film
23	second conductive thin film
25	silicon nitride layer
26	AlN thin film
51	Si substrate
52	LOCOS film
53	gate insulating film
54	gate electrode
54a	low resistant polysilicon layer
54b	silicide layer
55	insulating sidewall
56	low concentration source/drain region
57	high concentration source/drain region

【書類名】　図面
[Name of Document]　DRAWINGS

【図１】
[FIG. 1]



【図２】
[FIG. 2]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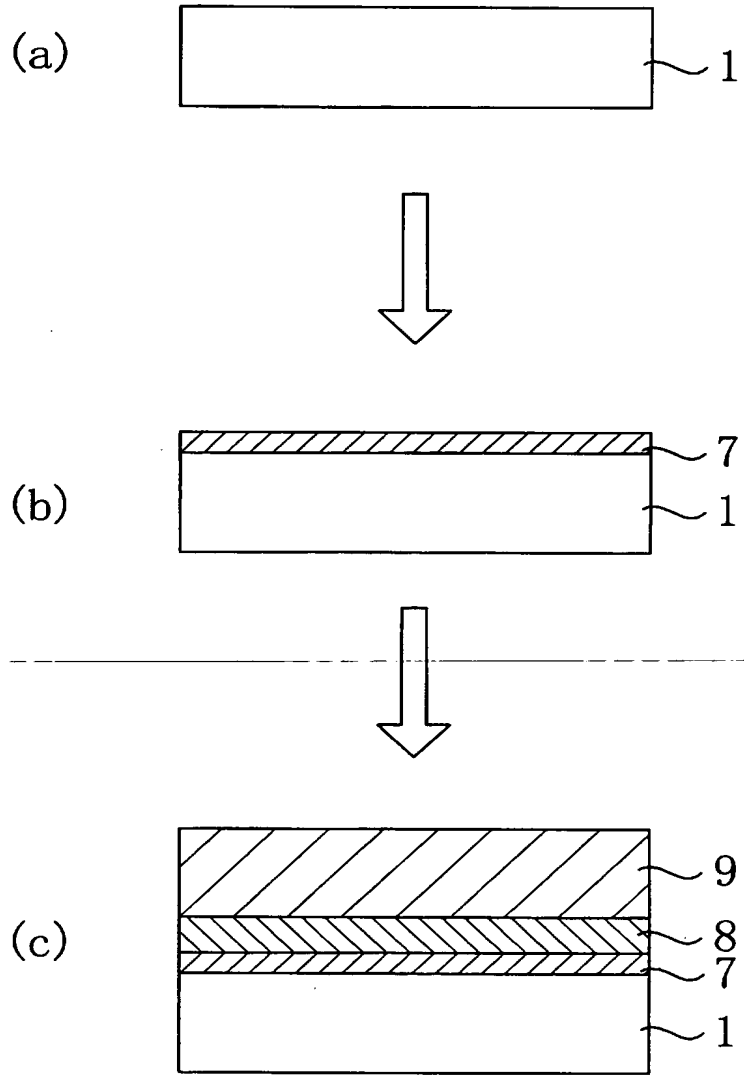
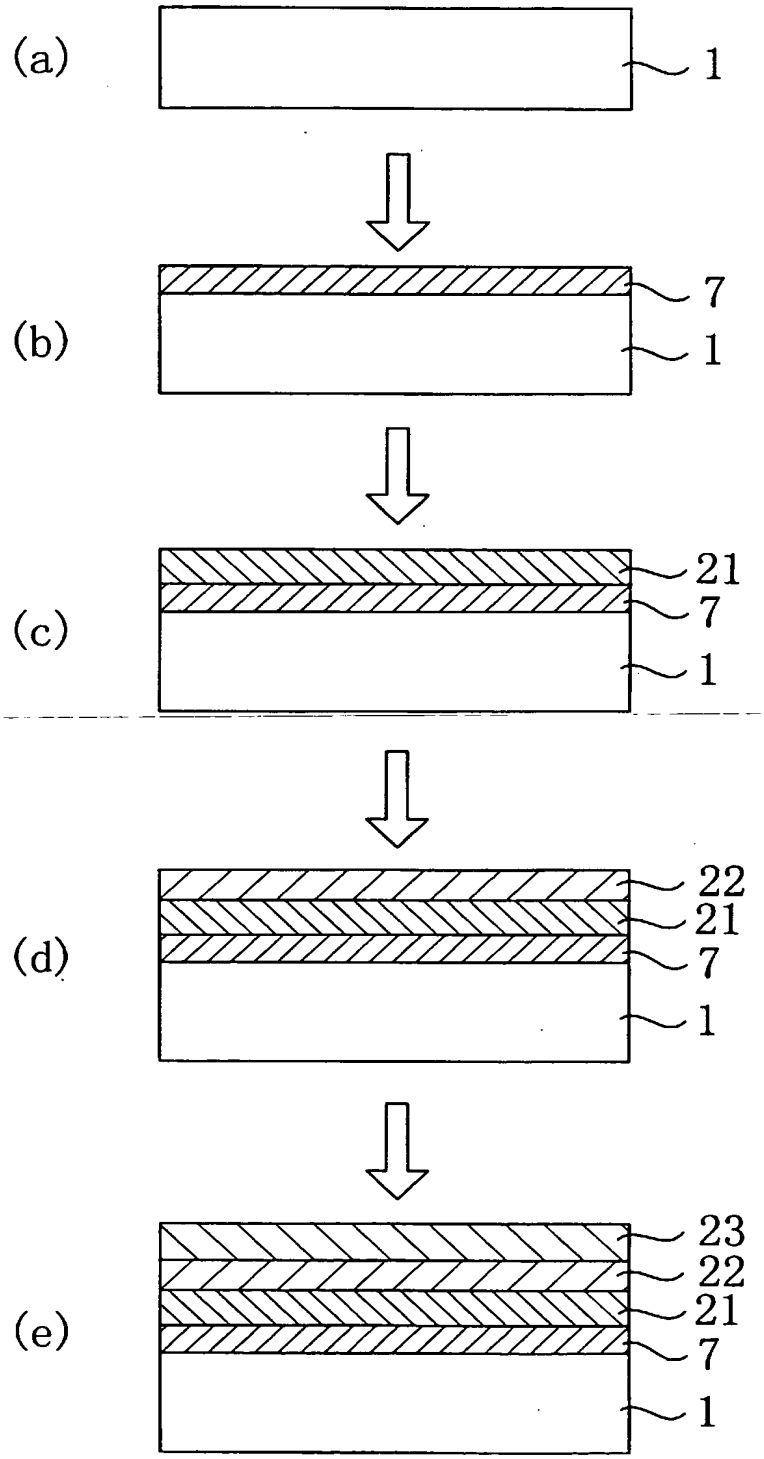
(b)
dangling bond
ダングリングボンド
2
1
termination chemical species
終端用化学種
(c)
11
2
1
(d)
12 終端原子
termination atom
1
N atom
N原子4
(e)
3
5a
12
1
Al atom
(f)
3Al原子
4
5b
12
1
(g)
AlN crystal layer
7 AlN結晶層
1

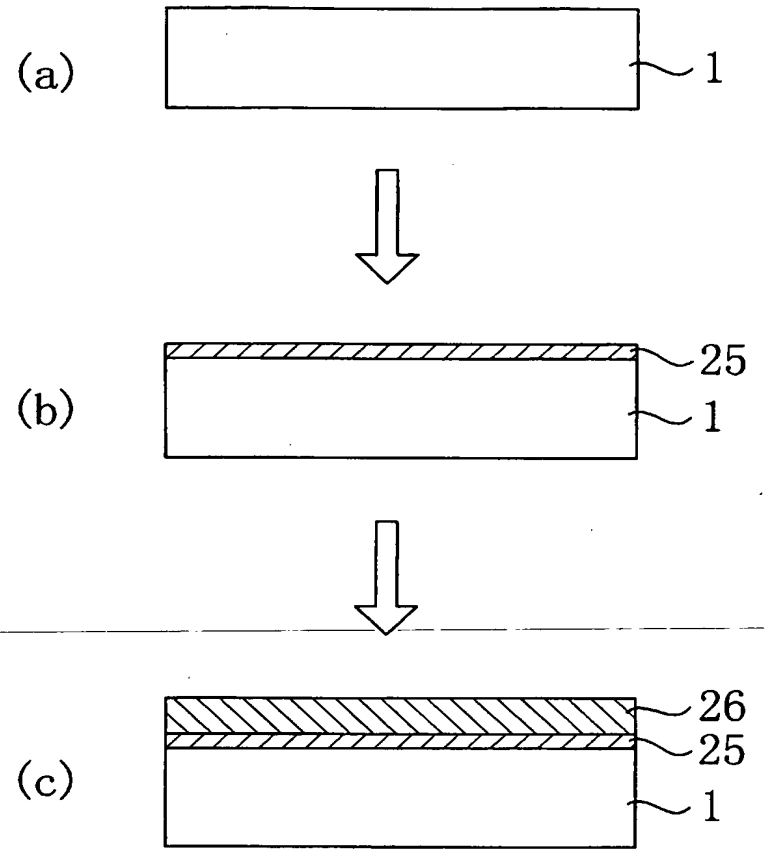
【図３】
[FIG. 3]



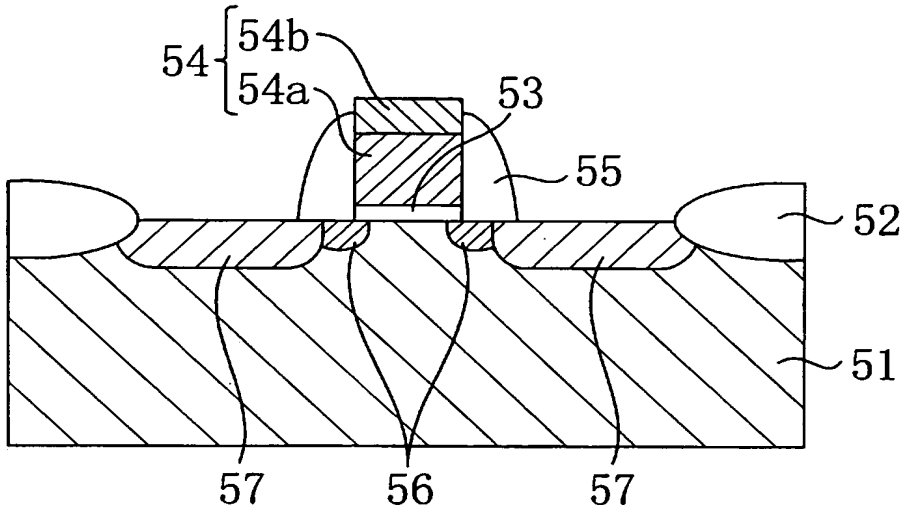
【図４】
[FIG. 4]



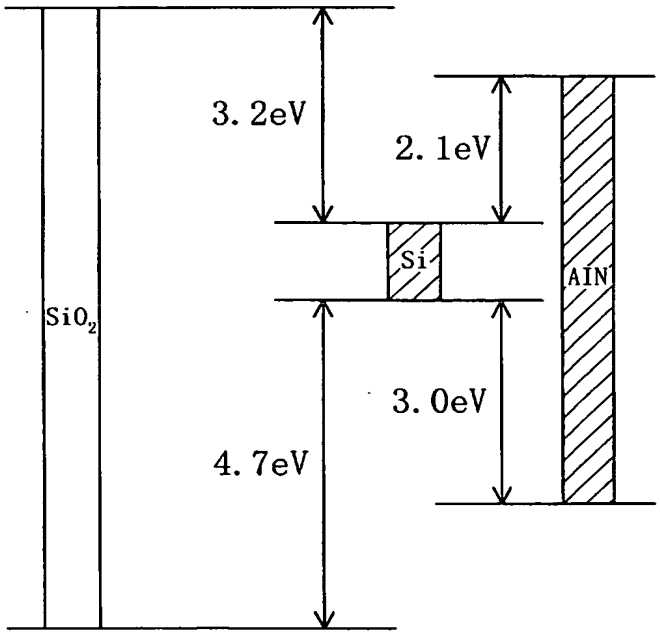
【図５】
[FIG. 5]



【図６】
[FIG. 6]



【図７】
[FIG. 7]



[Name of Document] Abstract

[Abstract]

[Purpose] To provide a method for fabricating a film which has high dielectric constant and good insulating properties and which can keep up with progress in the miniaturization and high integration of elements, and a semiconductor element making use of thereof.

[Solution] An Si substrate **1** is cleaned through acid treatment and heated to remove particles attached on the surface thereof. Then, when the surface of the Si substrate 1 is terminated by hydrogen atoms **10**, the hydrogen atoms **10** are left behind. While dangling bonds **2** are formed on the surface of the Si substrate **1**, these are terminated with chemical species **11**. As termination atoms **12** are left behind on the surface of the Si substrate **1**, with an MBE, for example, an N atoms layer and an Al atoms layer are alternatively stacked each by several tens layers to form an AlN crystal layer **7**. A compact crystalline AlN layer which has small interface states density and a higher dielectric constant than a silicon oxide film is used as a gate insulating film of a filed effect transistor or a capacity insulating film of a capacitor, thereby adopting to the miniaturization and high integration of elements.

[Selected Figure] FIG. **2**